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DATA SHEET

FUJITSU

MB90075

ON–SCREEN DISPLAY CONTROLLER FOR NTSC/PAL

DESCRIPTION

The MB90075 CMOS On–screen Display Controller (OSDC) is a peripheral LSI that displays 288 alphanumeric characters (24 rows x 12 lines) and figures on TV screen by a microcontroller. Since the MB90075 contains a character generator ROM (CGROM) which is capable to store 256 characters including special characters "Kanji characters" and "Kana characters", it can be used even for Japanese display, in addition to the standard alphanumeric display.

The MB90075 contains a video signal generator for NTSC/PAL system, so that the characters and figures can be displayed synthesizing with this internally generated video signal even no external video signal present. Also the MB90075 incorporates video signal analog switches to synthesize characters with a video signal.

Three video outputs are available on the MB90075; a composite video, a Y/C separate video, and a RGB digital outputs. Also the device has two video inputs; a composite video and a Y/C separate video inputs. The superimposed display function is possible at either composite video input or Y/C separate video input.

The MB90075 is fabricated by the silicon–gate CMOS process, and packaged in a 28–pin plastic shrink DIP (Suffix : P–SH) or 28–pin plastic SOP (Suffix : PF) package.

Because the MB90075 OSDC device has these powerful character display and control abilities, it is suitable for on–screen display on such applicable audio–video equipment as VCRs.

PRELIMINARY

MB90075–P–SH

28–PIN PLASTIC SH–DIP
(DIP–28P–M03)

MB90075–PF

28–PIN PLASTIC SOP
(FPT–28P–M02)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- Character display controller available for NTSC and PAL TV sets
- 24 rows x 12 lines screen format (Max. 288 characters/screen)
- 12 x 18–dot matrix high–quality character format
- 256–character set capability in character generator ROM (CGROM) (including the end code)
- Programmable display control
  - Character size : 1 width x 1 height or 2 widths x 2 heights per line
  - Character display position : 32 horizontal and 32 vertical positions
  - 8 kinds of color/monochrome for under–color/character by internal video signal generator
- Patterned (Bordered) or filled background character display
- On–chip display data RAM (VRAM)
- VRAM–fill function
- Analog Video Inputs
  - Composite video signal
  - Y/C separate video signal

FEATURES (Continued)

- Three-channel Video Output
  - Composite video signal
  - Y/C separate video signal
  - RGB digital signal
- On-chip video signal generator conforming to NTSC and PAL systems
- Separate or composite sync signal input/output
- 8-bit serial input to interface with microcontroller
- On-chip two clock generators
  - Display dot clock
  - Color burst clock
- Power-on reset function
- Single +5V power supply
- Wide operating temperature range: -30°C to +70°C
- Silicon-gate CMOS process
- Package options
  28-pin plastic shrink DIP (Suffix : P-SH)
  28-pin plastic SOP (Suffix : PF)

Figure 1. Pin Assignment

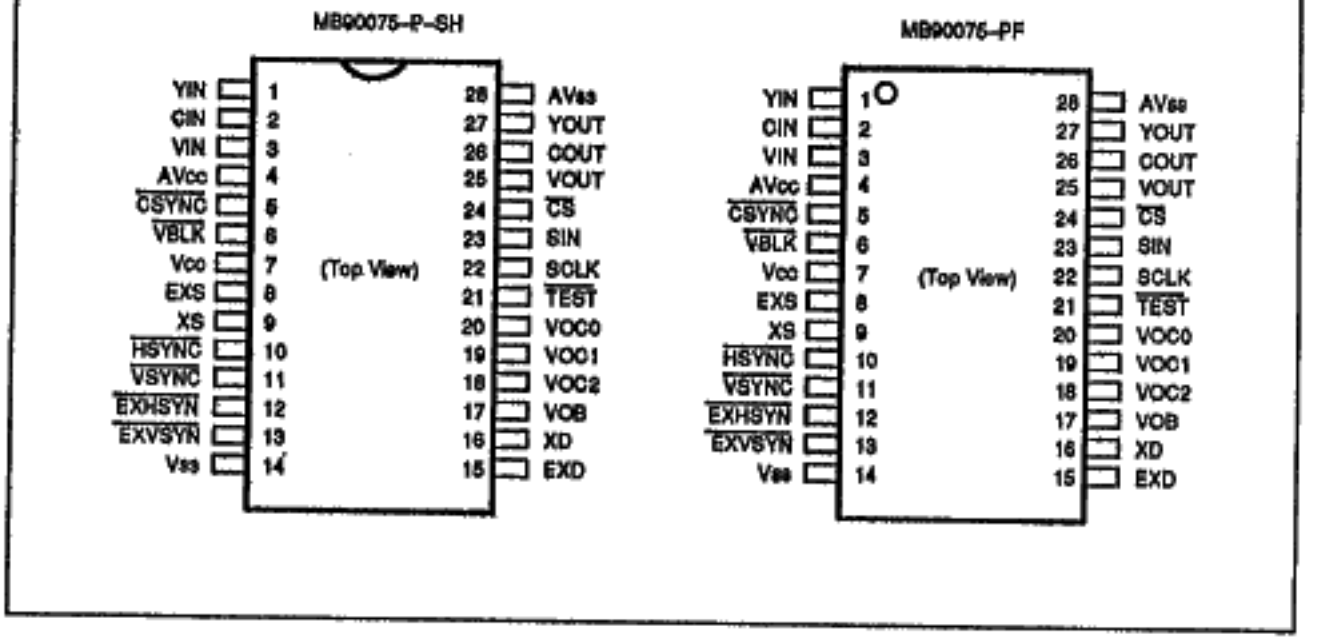
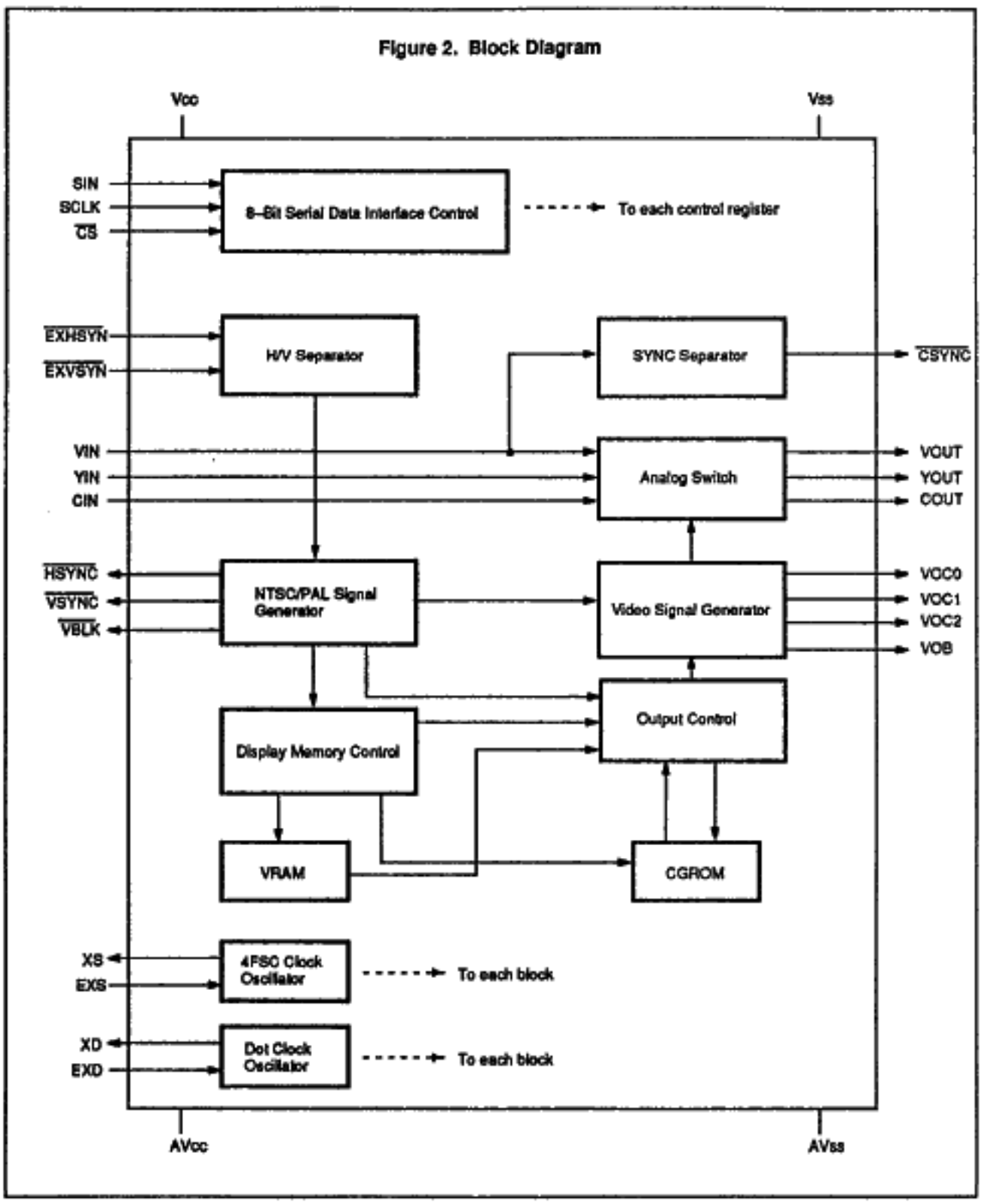


Figure 2. Block Diagram



PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB90075.

Table 1. Pin Description

Symbol	Pin No.	Type	Name & Function
Power Supply			
Vcc	7	–	Power supply pin for digital block
Vss	14	–	Ground pin for digital block
AVcc	4	–	Power supply pin for analog block. The voltage level applied to this pin must be the same as Vcc.
AVss	28	–	Ground pin for analog block. The ground level must be the same as Vss.
Clock			
EXS	8	I	Input to the internal oscillator running with an external crystal resonator and capacitors for color burst clock (NTSC: 14.31818MHz and PAL: 17.734475MHz).
XS	9	O	Output from the internal oscillator running with an external crystal resonator and capacitors for color burst clock (NTSC: 14.31818MHz and PAL: 17.734475MHz)
EXD	15	I	Input to the internal oscillator running with an external LC network circuit for display dot clock
XD	16	O	Output from the internal oscillator running with an external LC network circuit for display dot clock
Device Test			
$\overline{TEST}$	21	I	Test signal input pin. Normally, input a high level to this pin. When a low level is input, be sure not to issue commands.
Serial Interface			
$\overline{CS}$	24	I	Chip select pin. A low level on the $\overline{CS}$ pin activates serial data transfer to the device. (TTL level) Also, this pin can be used to release the power-on reset. This pin is hysteresis input and pulled up internally.
SIN	23	I	SIN is for serial data input. 8-bit serial data including command data and character data is input to this pin while the $\overline{CS}$ is active (TTL level). This pin is hysteresis input and pulled up internally.
SCLK	22	I	SCLK is for shift clock input to the internal register. At the rising edge of SCLK, data on the SIN pin is shifted into the LSB of an internal register and the contents of the internal register are shifted to MSB. (TTL level) The shifted data are latched into the 1-byte of internal latch circuit FIFO.
Analog I/O Port			
YIN	1	I	Luminance signal (Y-signal) input for the superimposed display. A DC-restored (DC-clamped) 2Vp-p signal with sync tip level = 1V and pedestal level = 1.57V is input to this pin.
CIN	2	I	Chroma signal (C-signal) input for the superimposed display. Input a signal with a DC 1.57V and color burst signal = 0.57Vp-p.
VIN	3	I	Composite video signal input for the superimposed display. Input a DC-restored (DC-clamped) 2Vp-p signal with sync tip level = 1V and pedestal level = 1.57V.

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Table 1. Pin Description (Continued)

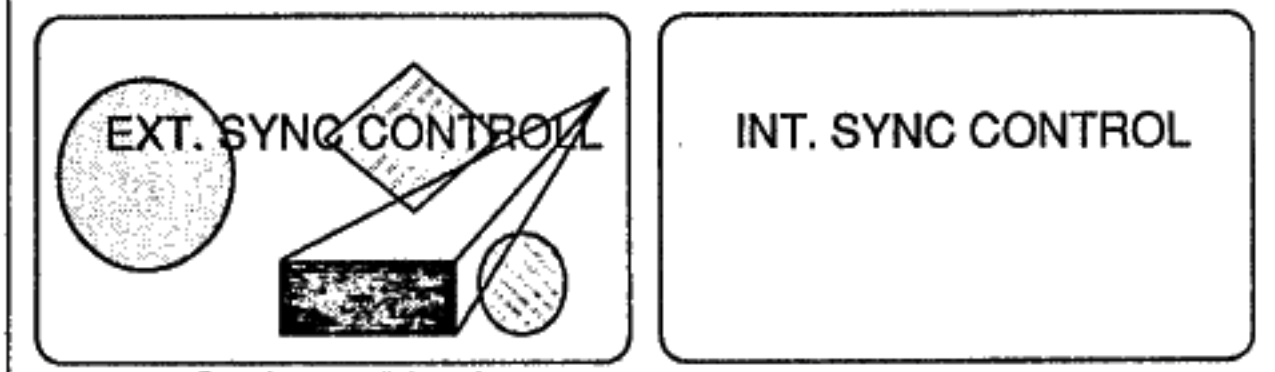
Symbol	Pin No.	Type	Name & Function
Analog I/O Port (continued)			
VOUT	25	O	Composite video signal output pin. This pin outputs 2Vp–p signal with sync tip level = 1V and pedestal level = 1.57V.
COUT	26	O	Chroma signal output pin. This pin outputs a signal with a DC 1.57V and a color burst =0.57Vp–p.
YOUT	27	O	Luminance signal output pin. This pin outputs 2Vp–p signal with sync tip level = 1V and pedestal level = 1.57V.
$\overline{VBLK}$	6	O	Vertical blanking signal output pin. This pin outputs a low level during the vertical blanking interval.
Output Port			
VOB	13	O	This is an character and its background signals output pin. (TTL level) While this pin outputs a high level, character and patterned or filled background information are output.
VOC2–VOC0	18–20	O	These are character signal output pins. (TTL level) These pins output a character color, character background color and under–color.
Sync Signal Related Port			
$\overline{CSYNC}$	5	O	Composite sync signal output pin. This signal is output after being separated from the composite video signal which is input to VIN pin.
$\overline{HSYNC}$	10	O	Horizontal sync signal output pin. This pin is also used for composite sync signal output. Furthermore, by forcing thr TEST pin low, it outputs a fsc clock.
$\overline{VSYNC}$	11	O	Vertical sync signal output pin. Also, by forcing thr $\overline{TEST}$ pin low, it outputs an oscillation clock for the dot clock.
$\overline{EXHSYN}$	12	I	External horizontal sync signal input pin. This pin is also used for composite sync signal input. This is a hysteresis input and internally pulled–up.
$\overline{EXVSYN}$	13	I	External vertical sync signal input pin. This is a hysteresis input and internally pulled–up.

DISPLAY FUNCTIONS

The MB90075 provides two types of screen display: external sync controlled operation and internal sync controlled operation. External sync controlled operation is used for the superimposed display of an externally input video signal and characters. Internal sync controlled operation is used to display characters after superimposing them with the internally generated video signal generated by the built-in video signal generator. In internal sync controlled operation, the MB90075 allows 8-color color display.

Figure 3 shows display examples in each video mode.

Figure 3. Video Modes



Note: For external sync controlled operation, characters are always displayed with monochrome gray scale.

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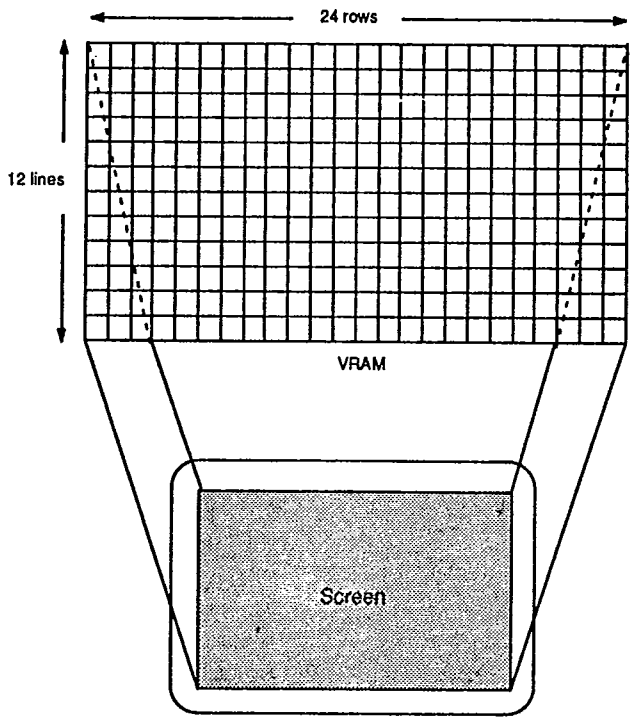
DISPLAY SCREEN CONFIGURATION

The MB90075 has a 288–character display memory (VRAM) so that when using the standard character size, it can display characters in up to 24 rows x 12 lines (= 288 characters) on one screen. When using enlarged characters, the number of characters that can be displayed on a screen is reduced depending on how much they are enlarged. Two character sizes (called standard size and enlarged size) can be set and specidfied either size for each line. So, the MB90075 can display characters of two different sizes together on the same screen. Figure 4 shows the display screen configuration.

Figure 4. Display Screen Configuration



CHARACTER CONFIGURATION

The MB90075 incorporates character generator ROM (CGROM) that can store up to 256 characters including the end code. Each character generated by CGROM consists of a 12 x 18 dot matrix.

Each character is displayed with a dot matrix consisting of 12 dots in the horizontal direction (row) and 18 dots in the vertical direction (line) as shown in Figure 5.

Also, two types of character size are available on MB90075: A standard size which consists of 12 x 18 dot matrix and an enlarged size which consists of (12 x 2) x (18 x 2) dot matrix. These two types of character size can be specified for each line on the screen. Figure 6 shows an example of character display with coexisting two types of size.

Figure 5. Character Dot Configuration

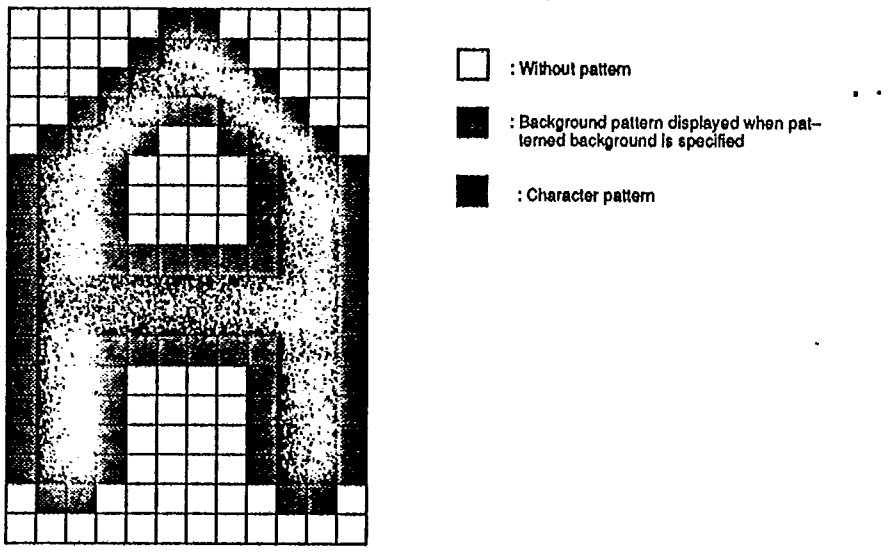


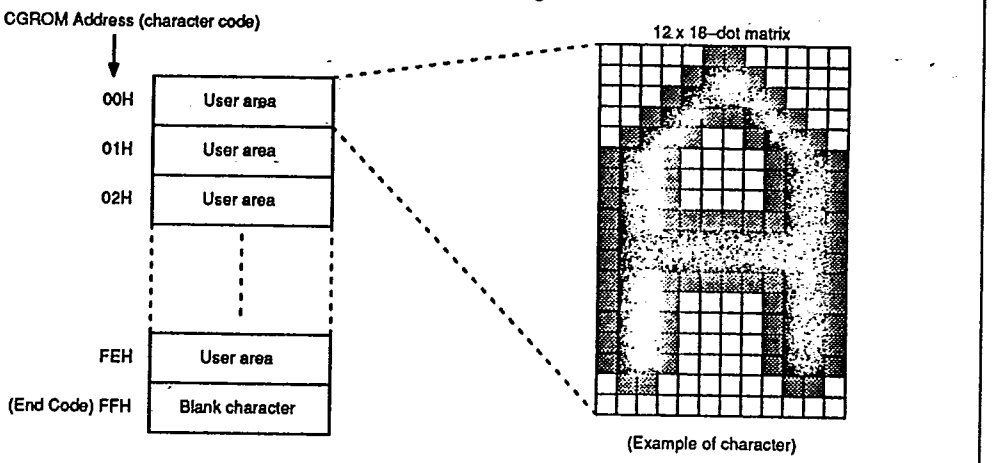
Figure 6. Example of Enlarged and Standard Size Characters Display

0 1 2 3 4 5 6 7 8 9 A B C D E F G H I J K L M N
O P Q R S T U V W X Y Z a b c d e f g h i j k l
m n o p q r s t u v w x y z 0 1 2 3 4 5 6 7 8 9
あいうえおかきくけこさしすせそたちつてとなにぬね
カセットテープ0 1 2 3 4
A B C D E F G H I J K L
M N O P Q R S T U V W X
日月火水木金土年週時分秒録画再生早送り巻戻し停止
ビデオタイマメモリカセットテープ0 1 2 3 4 5 6 7
Standard
Enlarged (double width x double height)
Standard

CONFIGURATION OF CGROM

The Character Generator ROM (CGROM) is configured with 12 dots horizontal x 18 dots vertical. It has a storage capacity for up to 256 character including the end code. The CGROM's address is corresponding to the character's code. Figure 7 shows the CGROM's configuration.

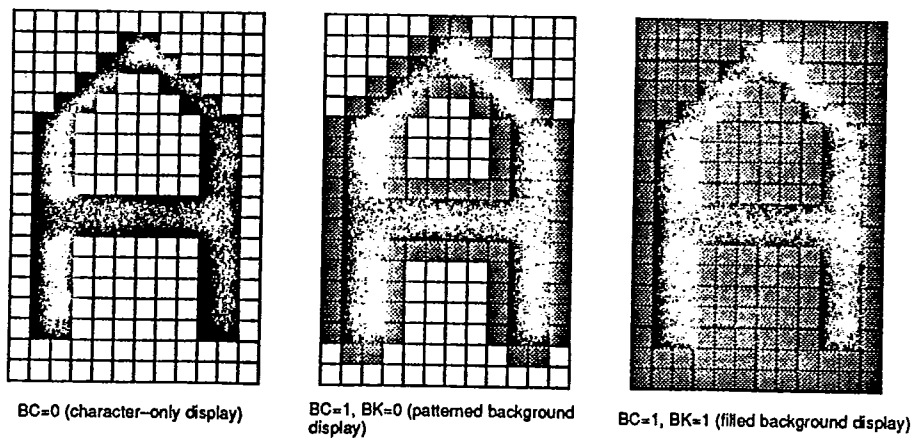
Figure 7. CGROM Configuration



CHARACTER DISPLAY FORMAT

The MB90075 allows to select a character display format from "character–only", "patterned background (border)", and "filled background" displays for each line by setting the internal registers (BC and BK bits set by command 6). Figure 8 shows an example for each of the character display formats.

Figure 8. Character Display Format



BC=0 (character–only display)

BC=1, BK=0 (patterned background display)

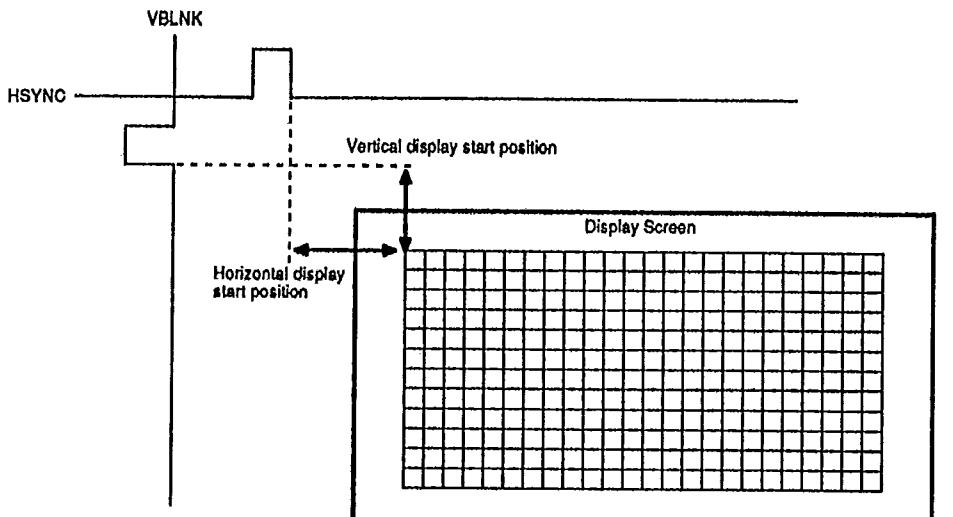
BC=1, BK=1 (filled background display)

CHARACTER DISPLAY START POSITION

The MB90075 allows to choose from 32 display start positions each in the horizontal and vertical directions by setting each internal register. By setting the appropriate display start positions depending on the screen configuration, you can arrange character placement so it is balanced across the screen.

To set the display start position of characters, specify the dot position at the upper left corner of the character at the upper left part of the screen. The display start position can be set in units of characters in the horizontal direction, and in units of two dots in the vertical direction. Figure 9 shows how the start position is specified in the horizontal and the vertical directions.

Figure 9. Character Display Start Position



DATA TRANSFER

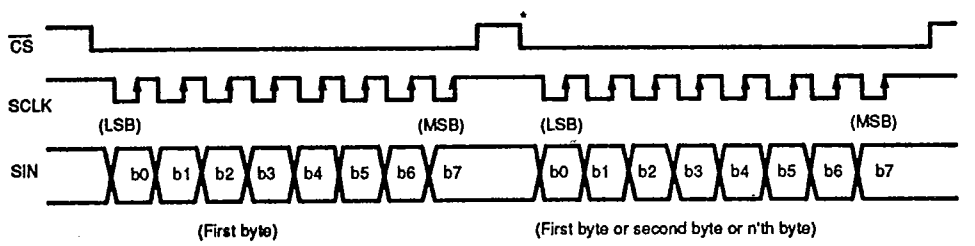
Display control commands and data are written to the MB90075 via 8–bit serial transfer block. This serial transfer is done by using three signals: $\overline{CS}$ (chip select), SCLK (shift clock), and SIN (serial data input). Figure 10 shows the timing of serial transfer. The $\overline{CS}$ pin is for the chip select signal, and is set Low for serial transfer. The SCLK pin is for the shift clock signal for data reception. The SIN pin is for the serial data input signal.

The data is eight bits length, and sequentially shifted into the SIN pin beginning with the least significant bit (LSB) . The data is latched and shifted in on each rising edge of the shift clock input to the SCLK pin as shown in Figure 10. The transferred data is loaded into the internal FIFO (First– In, First–Out) 1–byte buffer on the shift clock rising edge at the eighth bit. The data is read from FIFO and processed at times other than the display memory write period. Thus, commands and data can be written to the MB90075 at any time regardless of its display operation (i.e., asynchronously with display) by using the FIFO buffer.

In serial transfer, the number of received bits is counted by shift clock counts. Serial transfer may be reset by forcing the $\overline{CS}$ pin High; the reset can be cleared by driving the $\overline{CS}$ pin from High to Low, so that the subsequent eight bits of data (eight shift clock counts) are handled as byte data. In this way, byte synchronization can be maintained by using the $\overline{CS}$ pin.

If the $\overline{CS}$ signal goes High before eight bits of data are transferred, the data becomes invalid.

Figure 10. Serial Transfer Timing



* To maintain byte synchronization, the $\overline{CS}$ pin should be temporarily returned High before serial data transfer and set Low level to initiate data transfer.

CONTROL COMMANDS

The MB90075 control (display control) is done by writing data to the internal registers and display memory via serial data transfer. Table 2 lists the display control commands of the MB90075.

Table 2. Display Control Commands

Command No.	First Byte (Command ID code + Data)								Second Byte (Data)								Function
	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	
0	1	0	0	0	0	FL	A8	A7	0	A6	A5	A4	A3	A2	A1	A0	Preset VRAM address.
1	1	0	0	0	1	0	0	0	0	C2	C1	C0	0	B2	B1	B0	Set character and character background color
2	1	0	0	1	0	0	0	M7	0	M6	M5	M4	M3	M2	M1	M0	Write character code to VRAM.
3	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Reserved command.
4	1	0	1	0	0	IE	IN	0	0	0	CM	0	NP	0	0	DC	Control screen and sync.
5	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	Reserved command.
6	1	0	1	1	0	BK	G1	0	0	BC	VD	DG	N3	N2	N1	N0	Control character display in line.
7	1	0	1	1	1	EC	0	0	0	0	0	Y4	Y3	Y2	Y1	Y0	Set vertical display start position.
8	1	1	0	0	0	SC	0	0	0	0	0	X4	X3	X2	X1	X0	Set horizontal display start position.
9	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	Reserved command.
10	1	1	0	1	0	0	0	0	0	0	0	0	0	U2	U1	U0	Set under-color.
11	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Reserved commands.
12	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
13	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
14	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
15	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	

Notice that Reserved Commands (Command #3, 5, 9, 11, 12, 13, 14, and 15) are not effective for the device control. Do not issue these commands.

COMMAND DESCRIPTION

The following describes each command in detail and explains the operation.

Command 0 (Preset memory address)

[Function]

When writing character code and character color to the display memory (CVRAM), this command specifies the write address. The write address must be specified using this command before data can be written to VRAM by using command 2.

[Command format]

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
First byte	1	0	0	0	0	FL	A8	A7
	(MSB) 7	6	5	4	3	2	1	0 (LSB)
Second byte	0	A6	A5	A4	A3	A2	A1	A0

FL : VRAM–fill specification bit
A8–A0 : VRAM address bits

[Description]

The VRAM addresses are 9 bits length, and range from 000H to 177H. Addresses are specified by row (V) and column (H). The four high–order bits (A5–A8) are used to specify the row address, and the five low–order bits (A0–A4) are used to specify the column address within the row.

When FL bit = 1, VRAM–fill is done. VRAM–fill means to write the specified character codes into the VRAM address from the specified address to the last address. When FL = 0, VRAM–fill is not executed.

Also, VRAM address is automatically incremented by writing character code using command 2. character code is written to VRAM together with its character color character–by–character. VRAM–fill is executed by issuing command 2. *However, do not issue any command during the execution of VRAM–fill. VRAM–fill execution time is approximately 600μs to 1ms. (Valid sync signal input is required when operating under external sync control.)*

Though the VRAM addresses are non–contiguous, the address auto increment can be done by detecting free space in VRAM address to enable writing to contiguous addresses.

Command 1 (Character Grayscale(Color) Control)

[Function]

This command sets character grayscale (color) and character background grayscale (color) data.

[Command format]

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
First byte	1	0	0	0	1	0	0	0

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
Second byte	0	C2	C1	C0	0	B2	B1	B0

C2–C0 : Character grayscale (color) specification bits (for each character)
B2–B0 : Character background grayscale (color) specification bits (for each screen)

[Description]

The character grayscale (color) data specifies character grayscale or character color for video output and whether or not the character signal is output to the VOC2–VOC0 pins. This specification can be made for each character, and the data is written into VRAM and reflected in screen display by issuing command 2 (write character code). The character background grayscale data specifies character background grayscale for video output and whether or not the character background signal is output to the VOC2–VOC0 pins. When this command is issued, the character background grayscale for the entire screen is output as set.

C2, C1, C0 bits : These bits specify character grayscale (color).
B2, B1, B0 bits : These bits specify character background grayscale.

C2/ B2	C1/ B1	C0/ B0	Character signal output (for C2, C1, C1 bits)					Character background signal output (for B2, B1, B0 bits)				
			Digital output level			Video output		Digital output level			Video output	
			VOC2	VOC1	VOC0	Color	Monochrome	VOC2	VOC1	VOC0	Color	Monochrome
0	0	0	L	L	L	Black	Gray level 0 (Black)	L	L	L	Gray level 0 (Black)	Gray level 0 (Black)
0	0	1	L	L	H	Blue	Gray level 1	L	L	H	Gray level 1	Gray level 1
0	1	0	L	H	L	Red	Gray level 2	L	H	L	Gray level 2	Gray level 2
0	1	1	L	H	H	Magenta	Gray level 3	L	H	H	Gray level 3	Gray level 3
1	0	0	H	L	L	Green	Gray level 4	H	L	L	Gray level 4	Gray level 4
1	0	1	H	L	H	Cyan	Gray level 5	H	L	H	Gray level 5	Gray level 5
1	1	0	H	H	L	Yellow	Gray level 6	H	H	L	Gray level 6	Gray level 6
1	1	1	H	H	H	White	Gray level 7 (White)	H	H	H	Gray level 7 (White)	Gray level 7 (White)

Use CM bit of command 4 (Screen Control Register) to specify color/monochrome for video output. Note that video output for color display is only available when operating under internal sync control.

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Command 2 (Write character code)

[Function]

This command writes character code to the VRAM.

[Command format]

	(MSB)	7	6	5	4	3	2	1	0	(LSB)
First byte		1	0	0	1	0	0	0	M7	
	(MSB)	7	6	5	4	3	2	1	0	(LSB)
Second byte		0	M6	M5	M4	M3	M2	M1	M0	

M7–M0 : Character Code Specification Bits

[Description]

Command 2 sets the character code data. The data set in this register is written to the VRAM address specified by the write address register (command 0) along with the character grayscale (color) data (command 1). The character code is represented by eight bits from M7 to M0. The 256 kinds of character patterns 00H–FFH set in the internal CGROM can be used by setting these bits accordingly. When the data write operation is completed, the write address is automatically incremented.

Note : Write to VRAM is not executed during the HSYNC interval that the dot clock is idle. For this reason, if the HSYNC input is fixed low when operating under external sync control, no data can be written to VRAM. Also, notice that write to VRAM may not be executed if an unnecessary long period of HSYNC pulse is input. To ensure correct write to VRAM, set the HSYNC pulse width and the data transfer period (8–bit serial transfer time) so the equation below is met:

$\overline{\text{HSYNC}}$ Pulse width – 3 µs < 8–bit serial data transfer period

Command 4 (Control the Screen)

[Function]

This command exercises sync signal control and screen control.

[Command format]

	(MSB)	7	6	5	4	3	2	1	0	(LSB)
First byte		1	0	1	0	0	IE	IN	0	

	(MSB)	7	6	5	4	3	2	1	0	(LSB)
Second byte		0	0	CM	0	NP	0	0	DC	

IE : This bit specifies internal/external sync control.
IN : This bit specifies interlace/non-interlace control.
CM : This bit specifies color/monochrome display (video signal output).
NP : This bit specifies NTSC/PAL control.
DC : This bit specifies display control.

[Description]

When IE = 0, the device operates under internal sync control. The video signal output characters are displayed in color or grayscale (8 gray levels). The character background is output in grayscale (8 gray levels). The under-color, a background for the entire screen, is output in color or grayscale. Color display or grayscale display is specified by the CM bit.

When IE = 1, the device operates under external sync control. In this case, the video signal output and character background are displayed in grayscale. No under-color is output. Set the CM bit to 0. Otherwise, an unstable color like a rainbow will be displayed since the burst signal of external sync signal and the MB90075's chroma signal are asynchronous.

When IN = 0, it specifies interlace-scanned display. When 1, it specifies noninterlace-scanned display. However note that this specification is only valid under internal sync controlled operation.

When CM = 0, the video signal output when operating under internal sync control is displayed in monochrome, with character and under-color displayed in grayscale.

When CM = 1, the video signal output when operating under internal sync control is displayed in color (both characters and under-color). Note that set CM = 0 when operating under external sync control.

When NP = 0, the NTSC-standard signal is output. When 1, the PAL-standard signal is output. Note that this bit must be set correctly even when operating under external sync control.

When DC = 0, the device does not display for neither characters nor character background. It only display the under-color. (The under-color in video signal output is only displayed when operating under internal sync control.) When DC = 1, the device produces the display output.

Command 6 (Control Lines)

[Function]

This command controls character background and character enlargement for each line.

[Command format]

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
First byte	1	0	1	1	0	BK	G1	0

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
Second byte	0	BC	VD	DG	N3	N2	N1	N0

BK : Character background control bit
G1 : Character enlargement control bit
BC : Character background output bit
VD : Video output control bit
DG : Digital output control bit
N3–N0 : Line specification bit

[Description]

When BK = 0, it specifies a patterned background display. When 1, it specifies a filled background display.

When G1 = 0, it specifies standard character display. When 1, it specifies an enlarged character display where the character size is doubled.

When BC = 0, the device does not output the character background. When BC = 1, outputs the character background.

When VD = 0, the device does not output a character signal and character background signal to its video output pins (VOUT, YOUT, and COUT). When VD = 1, they are output to the video output pins (VOUT, YOUT, and COUT).

When DG = 0, the device does not output a character signal and character background signal to its digital output pins (VOC2–VOC0, and VOB). When DG = 1, they are output to the digital output pins (VOC2–VOC0, and VOB).

The N3–N0 bits correspond to the A8–A5 bits for the line address of VRAM address specification.

Command 7 (Set vertical display start position)

[Function]

This command controls synchronization and sets the display start position in the vertical direction.

[Command format]

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
First byte	1	0	1	1	1	EC	0	0

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
Second byte	0	0	0	Y4	Y3	Y2	Y1	Y0

EC : Control bit for sync signal output
Y0–Y4: Vertical display start position bits

[Description]

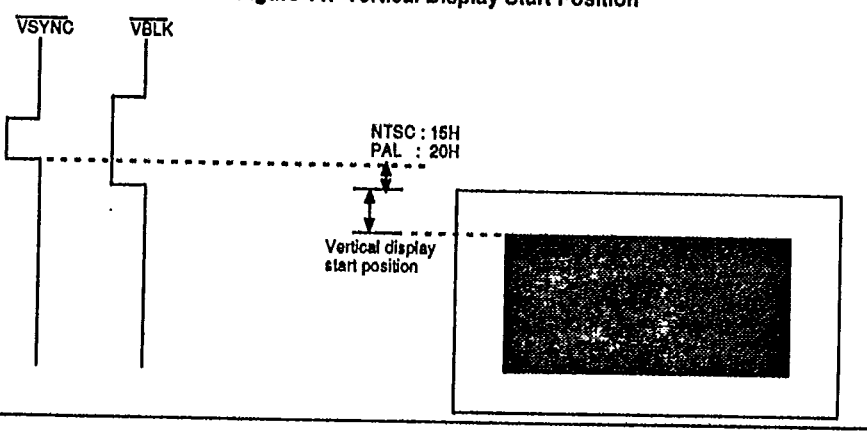
When EC = 0, the $\overline{HSYNC}$ pin outputs a composite sync signal. The $\overline{VSYNC}$ pin has its output level fixed. When EC = 1, the $\overline{HSYNC}$ pin outputs a horizontal sync signal. The $\overline{VSYNC}$ pin outputs a vertical sync signal.

Y4–Y0 set the vertical display start position. The vertical display start position can be set in the range from 00H to 1FH and can be moved in units of 2 dots. The position is given by the number of $\overline{HSYNC}$ low pulse after a high–going transition of the $\overline{VBLK}$ (vertical blanking) pulse.

Vertival Display Start Position = $Y4 \times 2^5 + Y3 \times 2^4 + Y2 \times 2^3 + Y1 \times 2^2 + Y0 \times 2^1 + 1$ (Unit : HSYNC)

Note : When Y4–Y0 are set to 0, the vertical display start position is 2H. The rising edge position of VBLK is 15H (for NTSC) or 20H (for PAL) after the rising edge of $\overline{VSYNC}$. Figure 11 shows the relationship between the vertical display start position vs. $\overline{VSYNC}$ and $\overline{VBLK}$.

Figure 11. Vertical Display Start Position



Command 8 (Set horizontal display start position)

[Function]

This command controls the sync signal and sets the horizontal display start positio

[Command format]

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
First byte	1	1	0	0	0	SC	0	0
	(MSB) 7	6	5	4	3	2	1	0 (LSB)
Second byte	0	0	0	X4	X3	X2	X1	X0

SC : Sync signal control bit
H0–H5: Horizontal display start position (00H–3FH)

[Description]

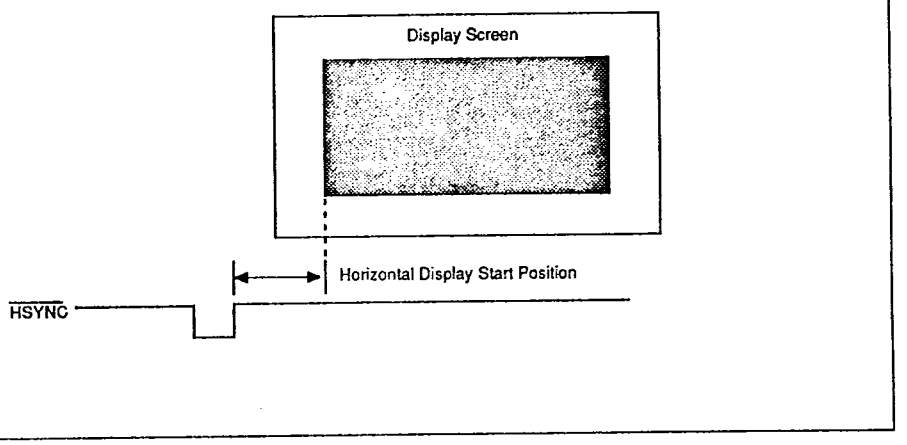
When SC = 0, the $\overline{\text{EXHSYN}}$ pin is set for composite sync signal input. So, the signal input to the $\overline{\text{EXVSYN}}$ pin is invalid. When SC = 1, the $\overline{\text{EXHSYN}}$ pin is set for horizontal sync signal input. The $\overline{\text{EXVSYN}}$ pin is set for vertival sync signal input.

The horizontal display start position can be set in the range from 00H to 1F and can be moved in units of characters. The start position is given by the number of dot clock pulses after the rising edge of $\overline{\text{HSYNC}}$.

Horizontal Display Start Position = $(X4 \times 2^4 + X3 \times 2^3 + X2 \times 2^2 + X1 \times 2^1 + X0 \times 2^0 + 15) \times 12$ (Unit : Dot CLock)

Figure 12 shows the relationship between the horizontal display start position and $\overline{\text{HSYNC}}$.

Figure 12. Horizontal Display Start Position



Command 10 (Control under-color)

[Function]

This command controls the under-color which is diplayed on a full-screen by internally generated video signal.

[Command format]

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
First byte	1	1	0	1	0	0	0	0

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
Second byte	0	0	0	0	0	U2	U1	U0

U2–U0 : The under-color (full-screen background color) specification bits

[Description]

U2–U0 bits specify the under-color (full-screen background color).

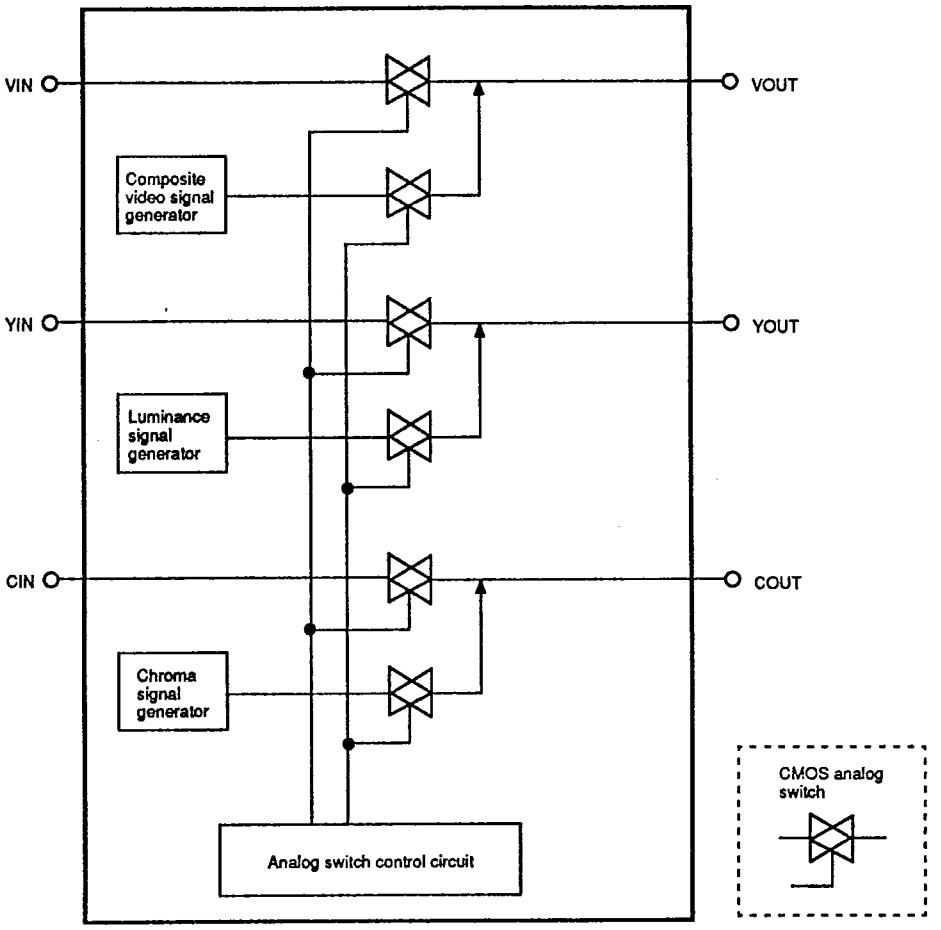
The under-color is displayed in areas other than those of characters and characters' background. The under-color of video output is only output when operating under internal sync control and is displayed in color or grayscale depending on the setting of CM bit with the command 4.

U2	U1	U0	Under-Color Output				
			Digital output level			Video output	
			VOC2	VOC1	VOC0	Color	Monochrome
0	0	0	L	L	L	Black	Gray level 0 (Black)
0	0	1	L	L	H	Blue	Gray level 1
0	1	0	L	H	L	Red	Gray level 2
0	1	1	L	H	H	Magenta	Gray level 3
1	0	0	H	L	L	Green	Gray level 4
1	0	1	H	L	H	Cyan	Gray level 5
1	1	0	H	H	L	Yellow	Gray level 6
1	1	1	H	H	H	White	Gray level 7 (White)

ANALOG SWITCH CIRCUIT

Figure 13 shows a functionally equivalent circuit of the analog switch section used to synthesize character information with an externally input or internally generated video signal.

Figure 13. Equivalent Circuit of Analog Switch Block



EXTERNAL SYNC CONTROL

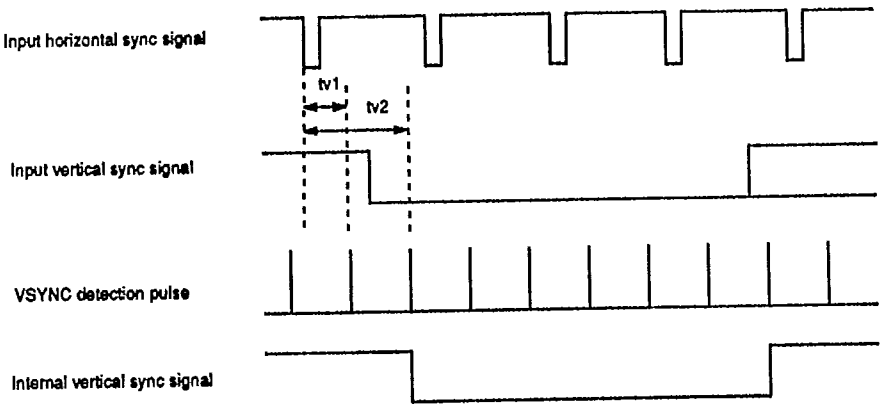
External sync control produces superimposed display by phase-synchronizing the MB90075's internal sync signal with an external sync signal. The external sync signal can be a H/V separate sync or a composite sync signal.

H/V Separate Sync Signal Input

By setting the SC bit to 1 by command 8, the $\overline{\text{EXHSYN}}$ pin can be used for horizontal sync signal input and the $\overline{\text{EXVSYN}}$ pin for vertical sync signal input, repectively. The $\overline{\text{EXHSYN}}$ pin contains a filter to cut signals below 3µs to eliminate noise and other unwanted components.

Vertical synchronization is detected by the internal VSYNC detection pulse. If a falling edge of the vertical sync signal occurs near this VSYNC pulse, a 1H delay may result, causing a vertical drift in character display. Figure 14 shows how the vertical sync is detected.

Figure 14. Vertical Sync Detect Operation



- For NTSC
  tv1 = 340 (4FSC clock) = approx. 23.8 µs
  tv2 = 796 (4FSC clock) = approx. 55.6 µs
- For PAL
  tv1 = 426 (4FSC clock) = approx. 24.0 µs
  tv2 = 994 (4FSC clock) = approx. 56.0 µs

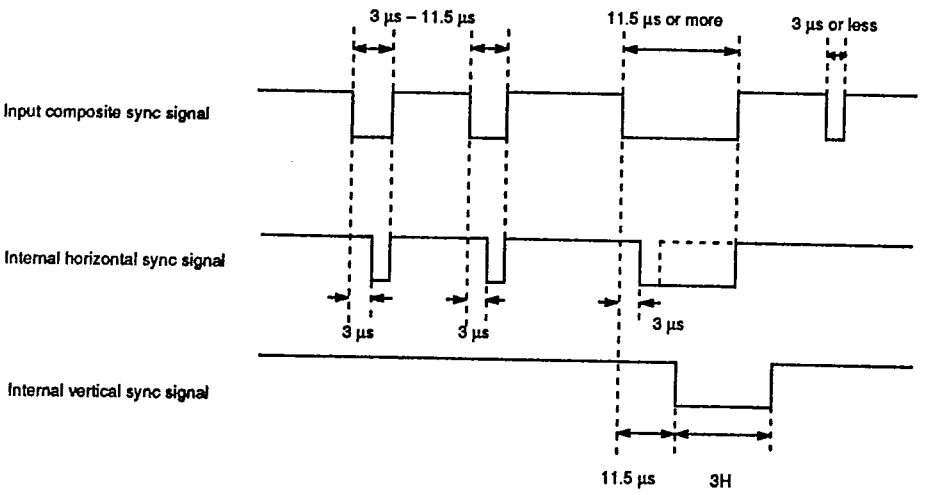
Composite Sync Signal Input

By setting the SC bit of the horizontal display start position register (command 8) to 0, the $\overline{\text{EXHSYN}}$ pin can be used for composite sync signal input.

Vertical synchronization is detected by measuring the pulse width of the signal input to the $\overline{\text{EXHSYN}}$ pin. When the pulse width of the signal input to the $\overline{\text{EXHSYN}}$ pin is equal to or greater than 11.5 µs, the signal is assumed to be the vertical sync pulse; when equal to or greater than 3 µs, it is assumed to be the horizontal sync pulse. Signals less than 3 us in pulse width are ignored as noise.

Figure 15 shows the internal timing of sync separate operation.

Figure 15. Internal Timing of Sync Separate Operation



Note: The exact value to determine whether or not a vertical sync pulse is 11.45 µs for NTSC and 11.50 µs for PAL.

- For NTSC,
  3 µs = approx. 45 (4FSC clock)
  11.45 µs = approx. 164 (4FSC clock)
- For PAL
  3 µs = approx. 57 (4FSC clock)
  11.50 µs = approx. 204 (4FSC clock)

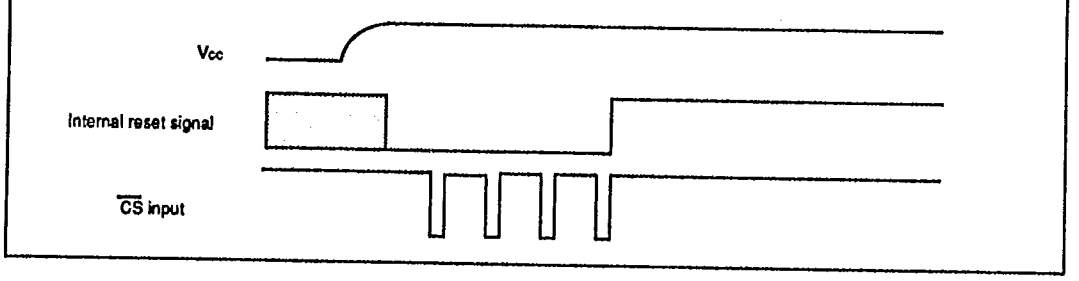
POWER–ON RESET

A power–on reset means that the device generates an internal reset signal to initialize its operation upon detection of power–on.

Input the $\overline{CS}$ signal four times to clear a power–on reset.

Figure 16 shows a timing of how a power–on reset is cleared.

Figure 16. Clearing Power–on Reset



DEVICE INITIALIZATION

When reset at power–on, the MB90075's screen control register has its IE (internal/external sync control) bit and DC (display control) bit cleared to 0, and screen display is turned off under internal sync control.

After power–on, clear a power–on reset first. Then, set the screen control register's DC bit to 1 to turn display on after setting all register data and all VRAM contents to be displayed.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Power Supply Voltage	Vcc	Vss–0.3		Vss+7.0	V	Make sure no different voltage level between AVcc and Vcc.
	AVcc	Vss–0.3		Vss+7.0	V	Make sure no different voltage level between AVcc and Vcc.
	AVss	Vss–0.3		Vss+7.0	V	Make sure no different voltage level between AVcc and Vcc. Should not exceed Vcc + 0.3V
Input Voltage	V_{IN}	Vss–0.3		Vss+7.0	V	Should not exceed Vcc + 0.3V
Output Voltage	V_{OUT}	Vss–0.3		Vss+7.0	V	Should not exceed Vcc + 0.3V
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	–30		+70	°C	
Storage Temperature	T_{STG}	–55		+150	°C	

NOTE : Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Power Supply Voltage	Vcc	4.5		5.5	V	Operation guaranteed range
	Vss		0			
	AVcc	4.5		5.5		Make sure no different voltage level between Vcc and AVcc.
	AVss		0			
Input High Voltage	V_{IHS}	0.8•Vcc		Vcc+0.3	V	
Input Low Voltage	V_{ILS}	Vss–0.3		0.2•Vcc	V	
Analog Input Voltage	AV_{IN}	0		Vcc	V	
Operating Ambient Temperature	T_A	–30		+70	°C	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

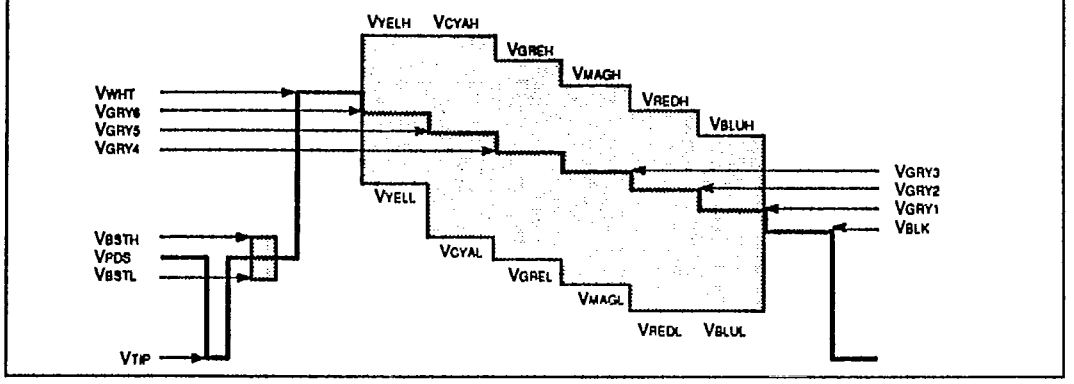
Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output High Voltage	V_{OH}	VOC2, VOC1, VOC0, VOB, $\overline{VBLK}$, $\overline{CSYNC}$, $\overline{HSYNC}$, $\overline{VSYNC}$	V_{CC}=4.5V I_{OH}=−200μA	2.4			V	
			V_{CC}=4.5V I_{OH}=−10μA	4.0			V	
Output Low Voltage	V_{OL}	VOC2, VOC1, VOC0, VOB, $\overline{VBLK}$, $\overline{CSYNC}$, $\overline{HSYNC}$, $\overline{VSYNC}$	V_{CC}=4.5V I_{OL}=3.2mA			0.6	V	
Input Current	I_{IL}	SIN, SCLK, $\overline{CS}$, $\overline{EXHSYN}$, $\overline{EXVSYN}$, $\overline{TEST}$	V_{CC}=5.5V V_{IL}=0.4V			−60	μA	
Supply Current	I_{CC}	V_{CC}, AVcc	V_{CC}=5.5V fc=4fsc=17.734475 MHz, fDC=8MHz Unloaded			60	mA	
ON resistance	R_{VON}	VIN–VOUT	V_{CC}=AVcc=4.5V I_{OL}=100μA			320	Ω	
	R_{YON}	YIN–YOUT	V_{CC}=AVcc=4.5V I_{OL}=100μA			320	Ω	
	R_{CON}	CIN–COUT	V_{CC}=AVcc=4.5V I_{OL}=100μA			320	Ω	
OFF Leakage Current	I_{VOFF}	VIN	V_{CC}=AVcc=5.5V V_{IN}=5.5V			10	μA	
	I_{YOFF}	YIN	V_{CC}=AVcc=5.5V Y_{IN}=5.5V			10	μA	
	I_{COFF}	CIN	V_{CC}=AVcc=5.5V C_{IN}=5.5V			10	μA	
Yellow Upper Level	V_{YELH}	V_{OUT}	V_{CC}=AVcc=5.0V	2.55	2.66	2.77	V	
Yellow Lower Level	V_{YELL}			2.18	2.29	2.40	V	
Cyan Upper Level	V_{CYAH}	V_{OUT}	V_{CC}=AVcc=5.0V	2.43	2.54	5.08	V	
Cyan Lower Level	V_{CYAL}			1.95	2.06	2.17	V	
Green Upper Level	V_{GREH}	V_{OUT}	V_{CC}=AVcc=5.0V	2.32	2.43	2.54	V	
Green Lower Level	V_{GREL}			1.89	2.00	2.11	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Magenta Upper Level	V_{MAGH}	V_{OUT}	Vcc=AVcc=5.0V	2.15	2.26	2.37	V	
Magenta Lower Level	V_{MAGL}			1.72	1.83	1.94	V	
Red Upper Level	V_{REDH}	V_{OUT}	Vcc=AVcc=5.0V	2.09	2.20	2.31	V	
Red Lower Level	V_{REDL}			1.60	1.71	1.82	V	
Blue Upper Level	V_{BLUH}	V_{OUT}	Vcc=AVcc=5.0V	1.86	1.97	2.08	V	
Blue Lower Level	V_{BLUL}			1.49	1.60	1.71	V	
Color Burst Upper Level	V_{BSTH}	V_{OUT}	Vcc=AVcc=5.0V	1.74	1.85	1.96	V	
Color Burst Lower Level	V_{BSTL}			1.18	1.29	1.40	V	
White Level	V_{WHT}	V_{OUT}	Vcc=AVcc=5.0V	2.38	2.54	2.70	V	
Black Level	V_{BLK}	V_{OUT}	Vcc=AVcc=5.0V	1.52	1.68	1.84	V	
Gray Level 1	V_{GRY1}	V_{OUT}	Vcc=AVcc=5.0V	1.64	1.80	1.96	V	
Gray Level 2	V_{GRY2}			1.75	1.91	2.07	V	
Gray Level 3	V_{GRY3}			1.87	2.03	2.19	V	
Gray Level 4	V_{GRY4}			2.04	2.20	2.36	V	
Gray Level 5	V_{GRY5}			2.15	2.31	2.47	V	
Gray Level 6	V_{GRY6}			2.27	2.43	2.59	V	
Pedestal Level	V_{PDS}	V_{OUT}	Vcc=AVcc=5.0V	1.49	1.57	1.65	V	
SYNC Level	V_{TIP}	V_{OUT}	Vcc=AVcc=5.0V	0.84	1.00	1.16	V	

Figure 17. Outputs on VOUT



DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

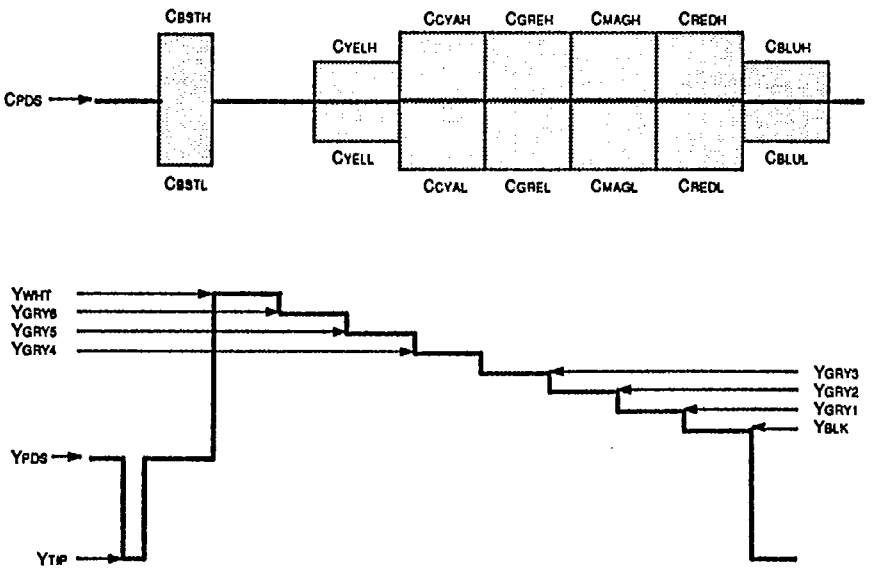
Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Yellow Upper Level	CYELH	COUT	VCC=AVCC=5.0V	1.63	1.74	1.85	V	
Yellow Lower Level	CYELL			1.29	1.40	1.51	V	
Cyan Upper Level	CCYAH	COUT	VCC=AVCC=5.0V	1.69	1.80	1.91	V	
Cyan Lower Level	CCYAL			1.23	1.34	1.45	V	
Green Upper Level	CGREH	COUT	VCC=AVCC=5.0V	1.69	1.80	1.91	V	
Green Lower Level	CGREL			1.23	1.34	1.45	V	
Magenta Upper Level	CMAGH	COUT	VCC=AVCC=5.0V	1.69	1.80	1.91	V	
Magenta Lower Level	CMAGL			1.23	1.34	1.45	V	
Red Upper Level	CREDH	COUT	VCC=AVCC=5.0V	1.69	1.80	1.91	V	
Red Lower Level	CREDL			1.23	1.34	1.45	V	
Blue Upper Level	CBLUH	COUT	VCC=AVCC=5.0V	1.63	1.74	1.85	V	
Blue Lower Level	CBLUL			1.29	1.40	1.51	V	
Color Burst Upper Level	CBSTH	COUT	VCC=AVCC=5.0V	1.74	1.85	1.96	V	
Color Burst Lower Level	CBSTL			1.18	1.29	1.40	V	
Pedestal Level	VPDS	COUT	VCC=AVCC=5.0V	1.49	1.57	1.65	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit	Remarks
				Min	Typ	Max		
White Level	Y_{WHT}	Y_{OUT}	V_{CC}=AVcc=5.0V	2.38	2.54	2.70	V	
Black Level	Y_{BLK}	Y_{OUT}	V_{CC}=AVcc=5.0V	1.52	1.68	1.84	V	
Gray Level 1	Y_{GRY1}	Y_{OUT}	V_{CC}=AVcc=5.0V	1.64	1.80	1.96	V	
Gray Level 2	Y_{GRY2}			1.75	1.91	2.07	V	
Gray Level 3	Y_{GRY3}			1.87	2.03	2.19	V	
Gray Level 4	Y_{GRY4}			2.04	2.20	2.36	V	
Gray Level 5	Y_{GRY5}			2.15	2.31	2.47	V	
Gray Level 6	Y_{GRY6}			2.27	2.43	2.59	V	
Pedestal Level	Y_{PDS}	Y_{OUT}	V_{CC}=AVcc=5.0V	1.49	1.57	1.65	V	
SYNC Level	Y_{TIP}	Y_{OUT}	V_{CC}=AVcc=5.0V	0.84	1.00	1.16	V	

Figure 18. Outputs on C_{OUT} and Y_{OUT}



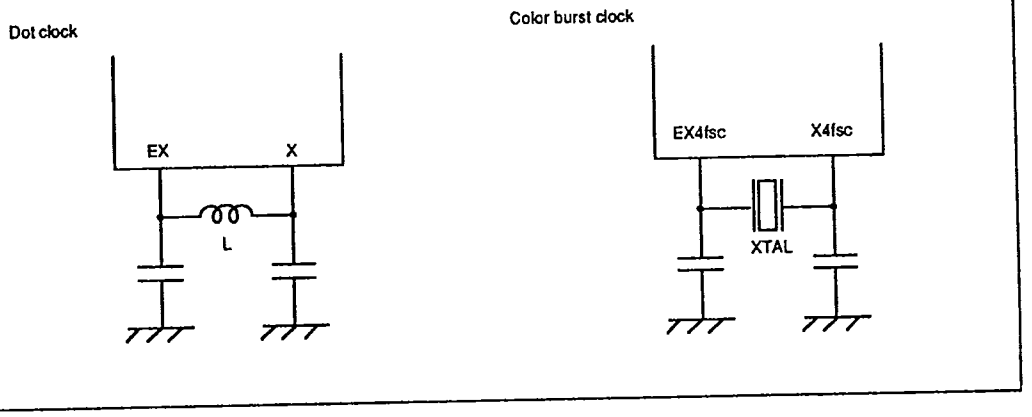
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Oscillator Characteristics

Parameter	Symbol	Pin/Port	Value			Unit	Remarks
			Min	Typ	Max		
Display Dot Clock Frequency	fdc	EXD, XD	6		8	MHz	Input signal with duty 50% is required.
Color Burst Clock Frequency	4fsc	EXS, XS		14.31818		MHz	Input signal with duty 50% is required. NTSC system
				17.734475		MHz	Input signal with duty 50% is required. PAL system

Figure 19. Clock Circuit Configuration



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Serial I/O Interface Timing

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ.	Max		
Shift Clock Cycle Time	t_{CYC}	SCLK	1000			ns	
Shift Clock Pulse Width	t_{WCH}	SCLK	450			ns	
	t_{WCL}		450			ns	
Shift Clock Rise Time	t_{CR}	SCLK			200	ns	
Shift Clock Fall Time	t_{CF}	SCLK			200	ns	
Shift Clock Start Time	t_{SS}	SCLK	200			ns	
Data Setup Time	t_{SU}	SIN	200			ns	
Data Hold Time	t_{H}	SIN	100			ns	
Chip Select End Time	t_{EC}	$\overline{CS}$	500			ns	
Chip Select Rise Time	t_{CRC}	$\overline{CS}$			200	ns	
Chip Select Fall Time	t_{CFC}	$\overline{CS}$			200	ns	
Horizontal Sync Rise Time	t_{HR}	$\overline{EXHSYN}$			200	ns	
Horizontal Sync Fall Time	t_{HF}	$\overline{EXHSYN}$			200	ns	
Vertical Sync Rise Time	t_{VR}	$\overline{EXVSYN}$			200	ns	
Vertical Sync Fall Time	t_{VF}	$\overline{EXVSYN}$			200	ns	
Horizontal Sync Signal Pulse Width	t_{WH}	$\overline{EXHSYN}$	4.4		5.0	µs	When H/V separate sync signals are input.
Vertical Sync Signal Pulse Width	t_{WV}	$\overline{EXVSYN}$	1		5	H	When H/V separate sync signals are input.
Horizontal Sync Signal Detective Pulse Width	t_{WCSH}	$\overline{EXHSYN}$	4.4		5.0	µs	When H/V composite sync signal is input.
Vertical Sync Signal Detective Pulse Width	t_{WCSV}	$\overline{EXVSYN}$	13		28	µs	When H/V composite sync signal is input.

Figure 20. Data Transfer Timing

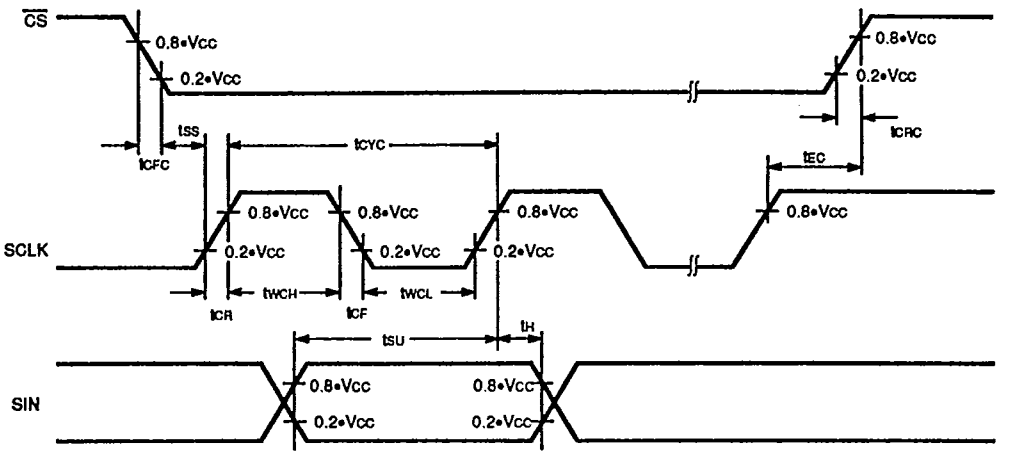


Figure 21. Shift Clock Hold Timing

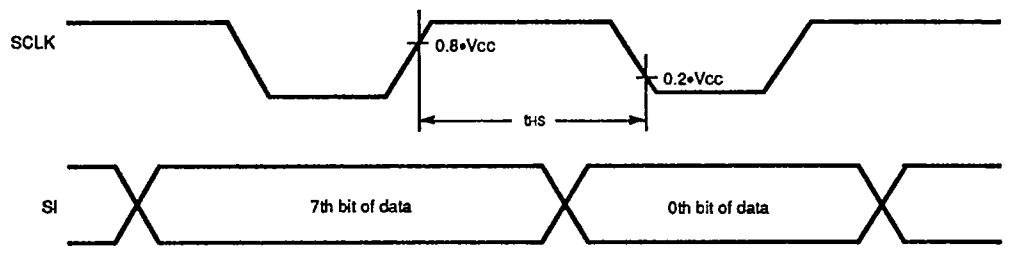


Figure 22. External Sync Signal Input Timing

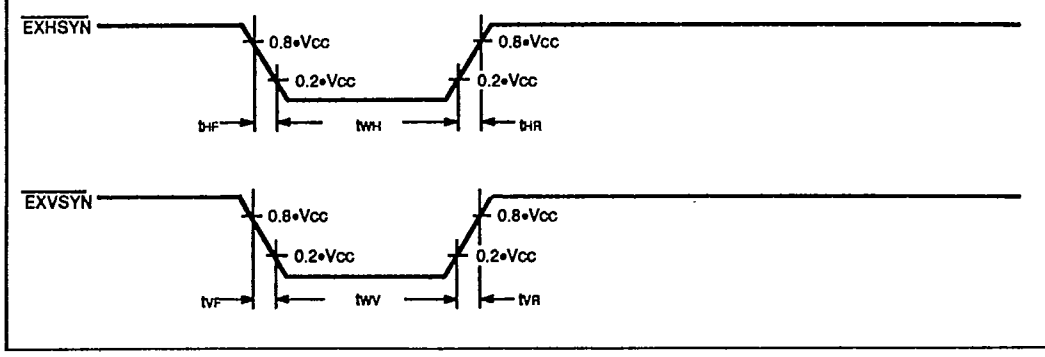
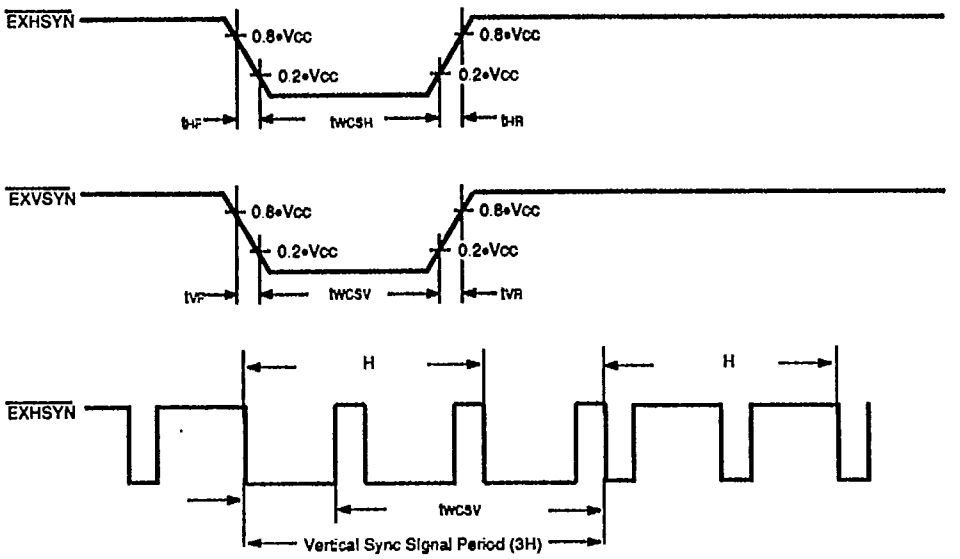


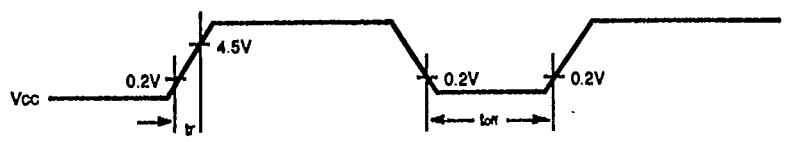
Figure 23. External Composite Sync Signal Input Timing



Power–On Reset Timing

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power Supply Rising Time	tr	0.05	50	ms	Required for the operation of the power–on reset circuit
Power Supply Shut–off Time	toff	1.0	–	ms	Required for the accurate circuit operation repeatly.

Figure 24. Power–On Reset Timing



Power supply should be raised smoothly.

RECOMMENDED EXTERNAL SYNC SIGNAL INPUT TIMING

Composite Sync Signal Input Timing

Parameter	NTSC	PAL	Unit	Remarks
Number of frame scanning lines	525	625	H	Note 1
Field frequency	59.94	50	Hz	
Line frequency	15734.264	15625	Hz	
Vertical blanking interval	19 to 21	25	H	Note 1
First equalizing pulse interval	3	2.5	H	Note 1
Vertical sync pulse interval	3	2.5	H	Note 1
Second equalizing pulse interval	3	2.5	H	Note 1
Equalizing pulse width	2.29 to 2.54	2.35 ± 0.1	µs	
Equalizing pulse period	0.5	0.5	H	Note 1
Serrated pulse width	3.81 to 5.34	4.7 ± 0.2	µs	
Serrated pulse period	0.5	0.5	H	Note 1
Horizontal sync signal period	63.5555	64	µs	
Horizontal sync signal pulse width	4.7 ± 0.1	4.7 ± 0.2	µs	
Horizontal blanking time	10.5 to 11.4	12 ± 0.3	µs	

Note 1: H is counted in units of horizontal sync signal periods (i.e., 1H = one horizontal sync signal period).

H/V Separation Sync Signal Input Timing

Parameter	NTSC	PAL	Unit	Remarks
Vertical sync signal frequency	59.94	50	Hz	
Vertical sync signal pulse width	1 to 5	1	H	Note 1
Horizontal sync signal period	63.5555	64	µs	
Horizontal sync signal pulse width	4.7 ± 0.1	4.7 ± 0.2	µs	

Note 1: Figures in ( ) are for color display.
Note 2: H is counted in units of horizontal sync signal periods (i.e., 1H = one horizontal sync signal period).

INTERNAL SYNC SIGNAL OUTPUT TIMING

Horizontal Timing

Parameter	NTSC Standard	PAL Standard	Unit	Remarks
HPS	0	0	4•fsc Clock	See Figure 25.
EP1E	35	42	4•fsc Clock	
HPE	68	84	4•fsc Clock	
HBSTS	76	100	4•fsc Clock	
HBSTE	112	140	4•fsc Clock	
HBLKE	136	186	4•fsc Clock	
SP1S	388	484	4•fsc Clock	
EP2S	455	568	4•fsc Clock	
EP2E	490	610	4•fsc Clock	
SP2S	842	1050	4•fsc Clock	
HBLKS	888	1106	4•fsc Clock	
HPS	910	1135 (1137)*	4•fsc Clock	

* : The value in the parentheses is applied at the final raster.

Vertical Timing

Parameter	NTSC Standard		PAL Standard		Unit	Remarks
	Interlaced	Non-Interlaced	Interlaced	Non-Interlaced		
VPS	0	0	0	0	0.5H	
VPE	6	6	5	5	0.5H	
EQPE	12	12	10	10	0.5H	
VBLKE	36	36	45	45	0.5H	
VBLKS	519	519	620	620	0.5H	
VPS	525	526	625	626	0.5H	

The 0.5H in the above table indicate the count values of 1/2H on the horizontal sync signal.

Figure 25. NTSC/PAL Horizontal Timing

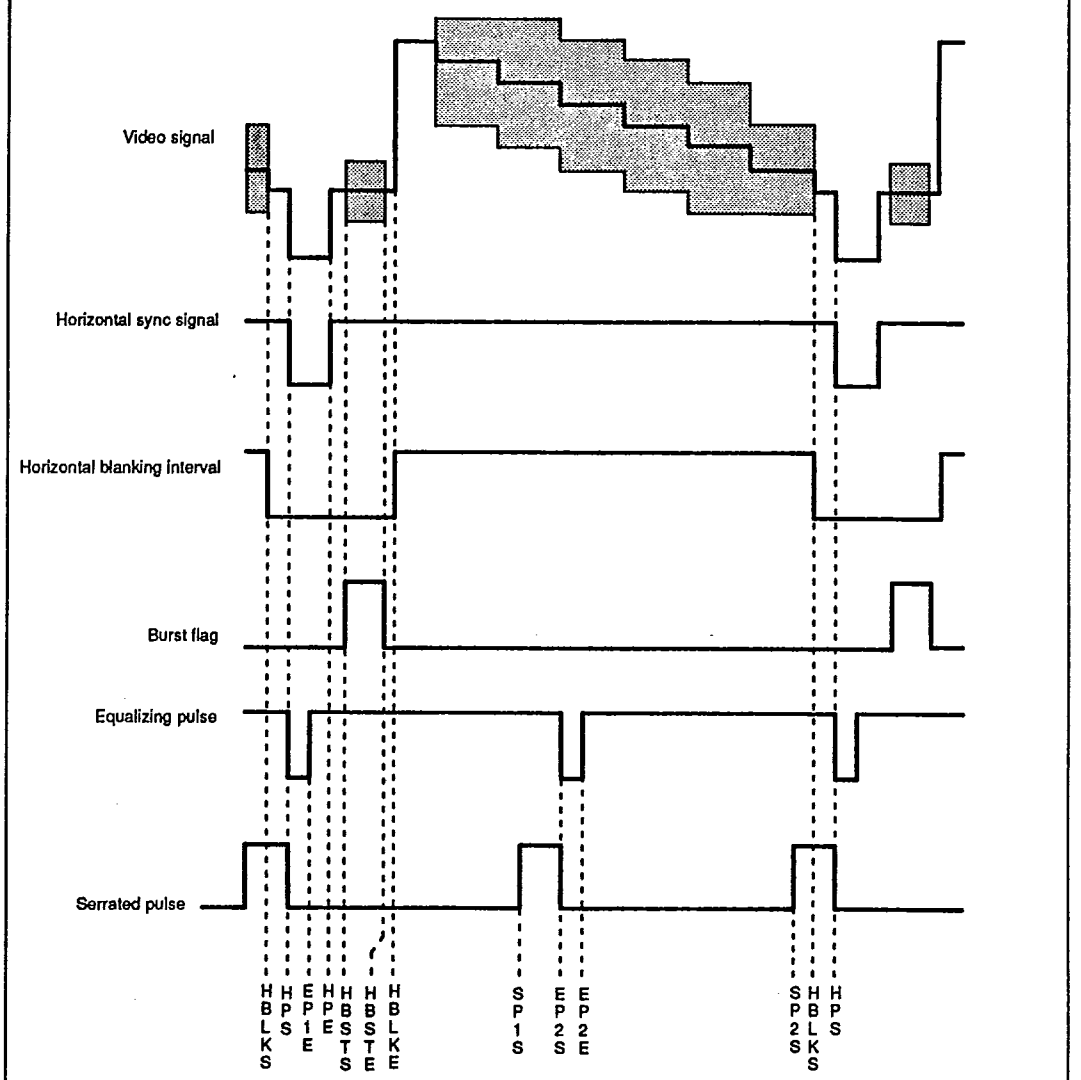


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Figure 26. NTSC Vertical Timing

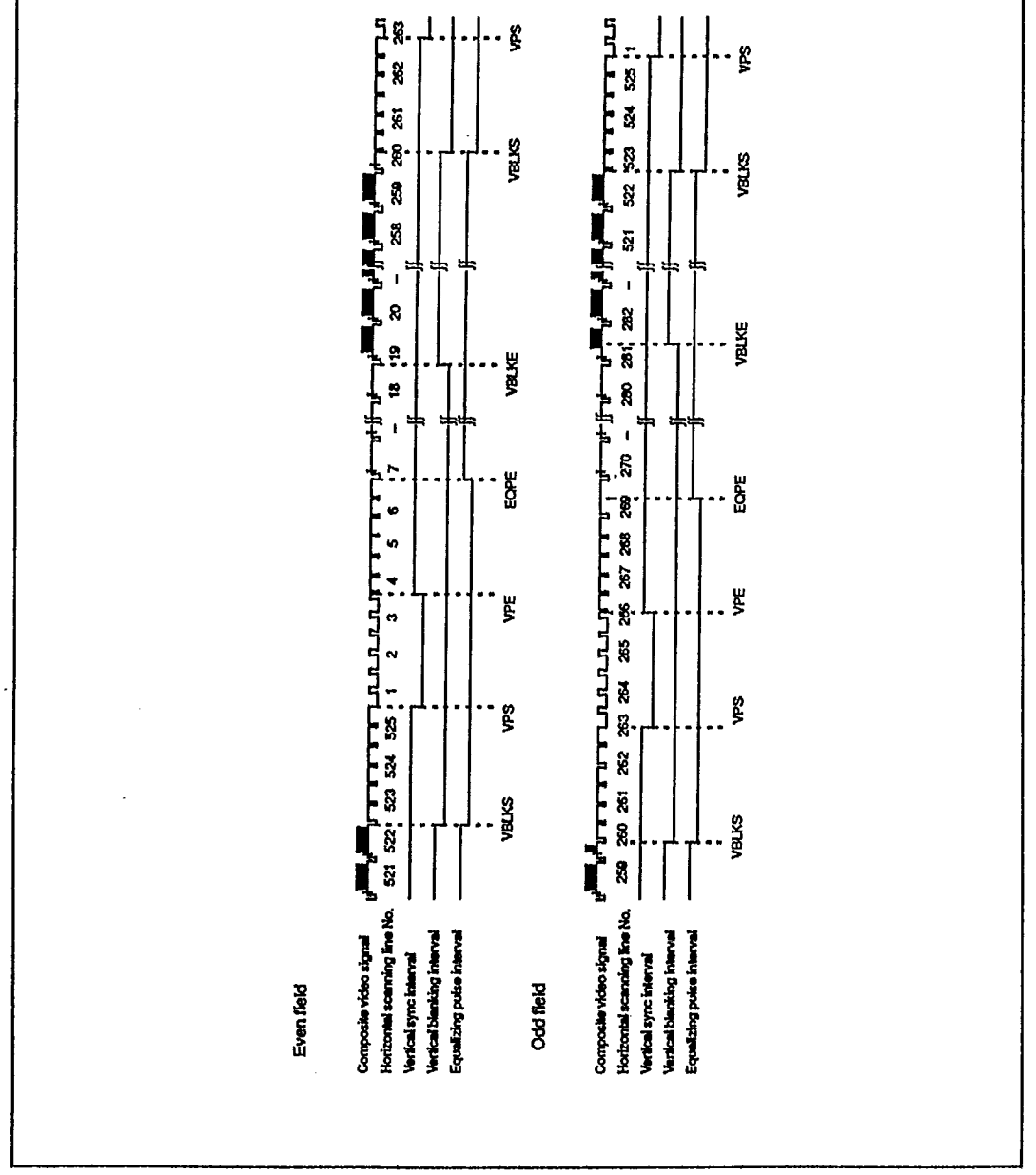

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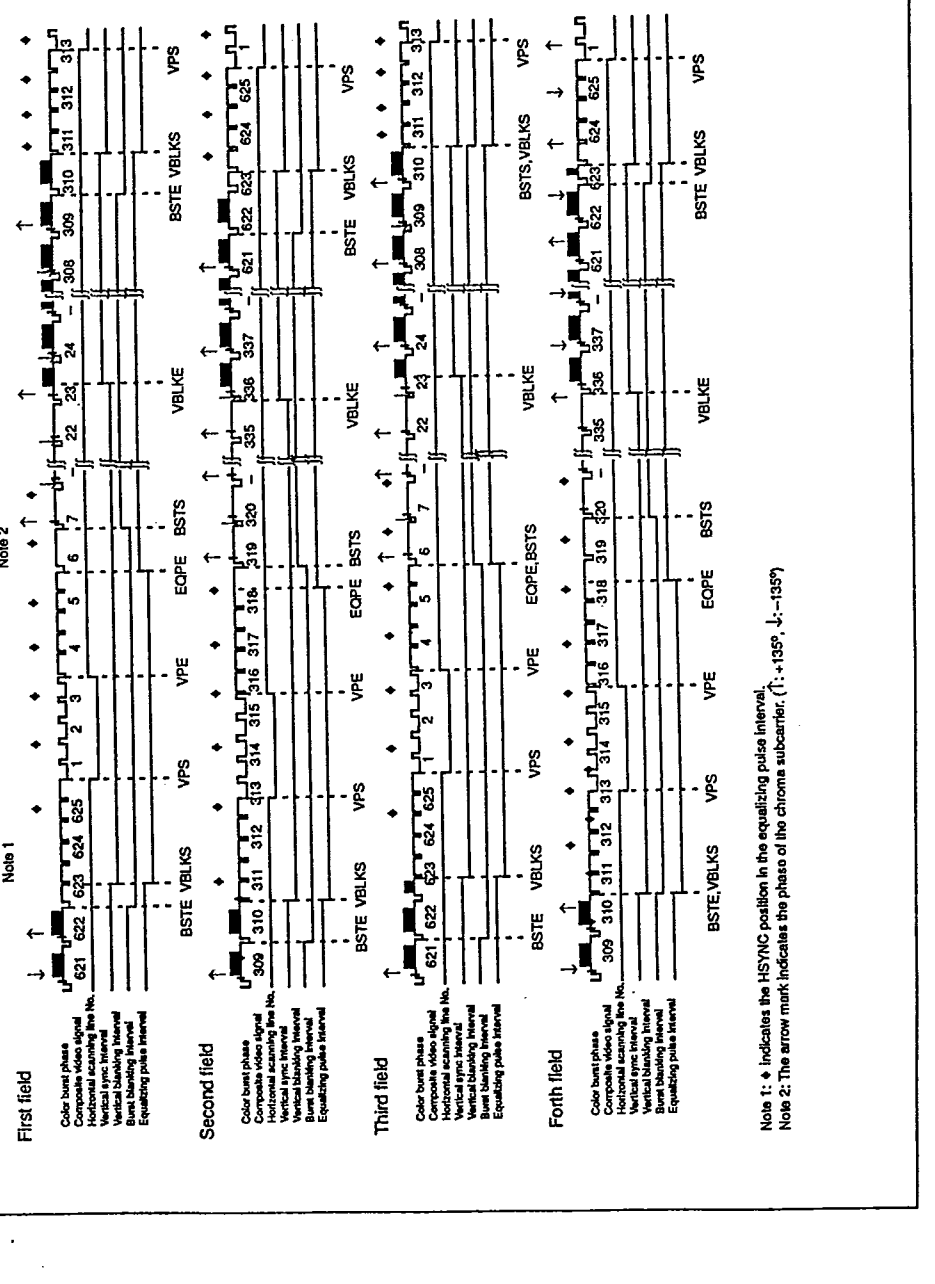
Figure 27. PAL Vertical Timing

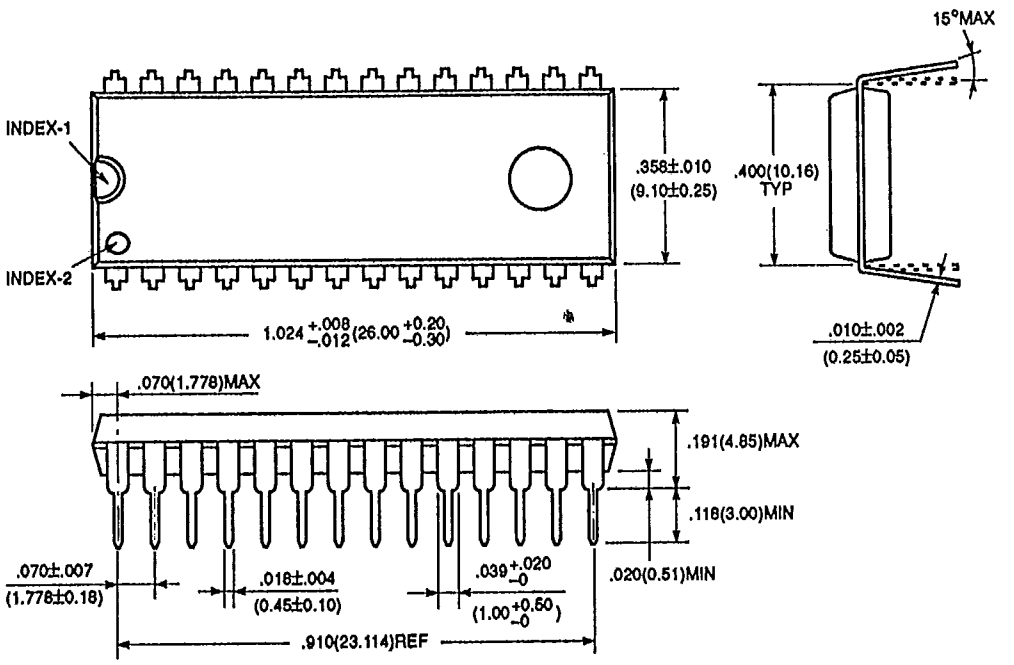


Note 1: ◆ indicates the HSYNC position in the equalizing pulse interval.
Note 2: The arrow mark indicates the phase of the chroma subcarrier. (↑: +135°, ↓: −135°)

PACKAGE DIMENSIONS

MB90075P-SH

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M03)



Dimensions in
inches (millimeters)

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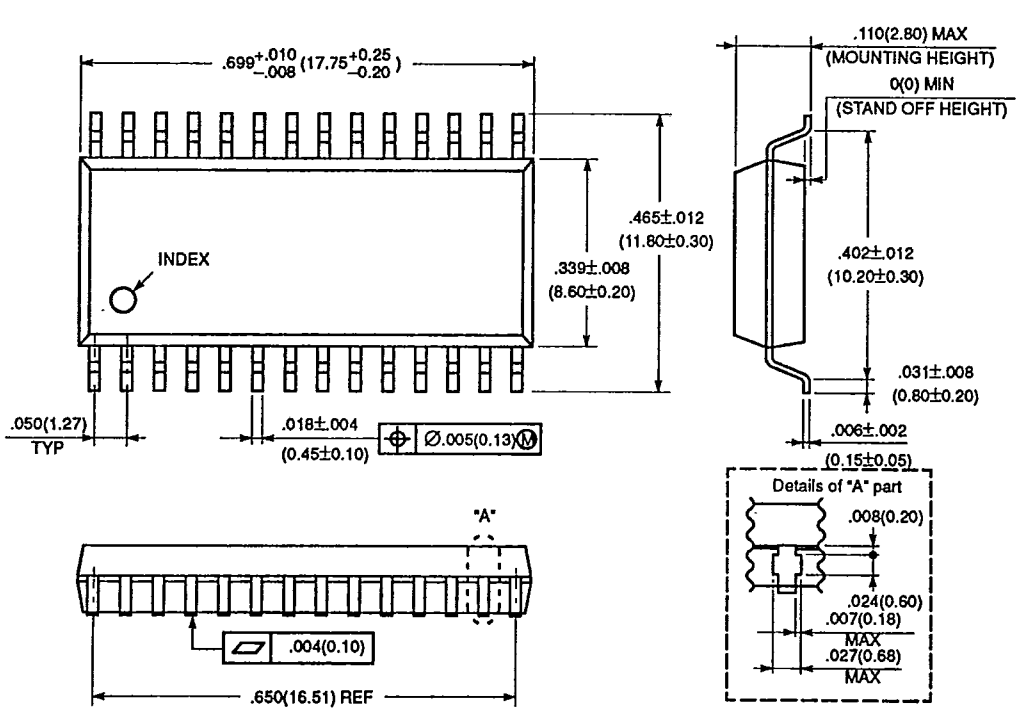
T-52-33-47

MB90075PF

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M02)



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Dimensions in
inches (millimeters)

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